MEC^2

Multi-channel Echo Canceller Card

Reference Design

Revision 1.0

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General

The document describes the reference design of hardware Multi-channel Echo Canceller Card (MEC²). MEC² is a low cost, high-performance Blackfin Ô DSP module performing simultaneous echo cancellation and speech enhancement on several communication channels in VoIP applications such as VoIP PBX, gateways and others.

MEC² is powered by Alango Voice Communication Package of digital signal processing technologies including:

- **echo cancellation**
- **noise suppression**
- **automatic gain control and dynamic range compressor**

MEC² reference design is highly configurable allowing its customization for different applications. For example, due to pin-compatibility of BF531/2/3 processors, the right (cheapest) processor may be chosen according to the number of channels processed for a specific customer application.

1 MEC² block diagram

MEC2 block diagram is illustrated on Figure 1.

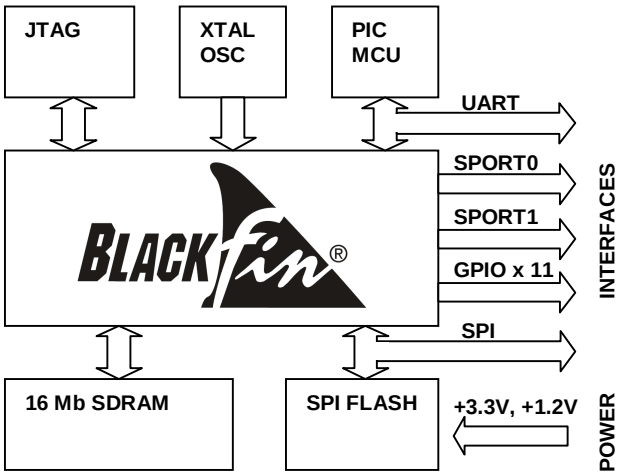

Figure 1. MEC² Functional Block Diagram

MEC² integrates Analog Devices Blackfin DSP BF531/2/3, 25MHz crystal oscillator, 16 Mbytes SDRAM, 128M byte serial SPI flash, and PIC16F54 Microchip microcontroller (see Fig. 1). The board is linked to system circuit by 40 pins connector. The pin diagram is shown on Fig. 2. It contains two symmetrical multi-channel PSM (SPORT) buses, SPI for control and serial flash memory programming, UART for debug purpose, 11 GPIO lines, and power supply lines. The MEC² card also integrates JTAG connector that can be used as a debug tool or an alternative flash programming tool.

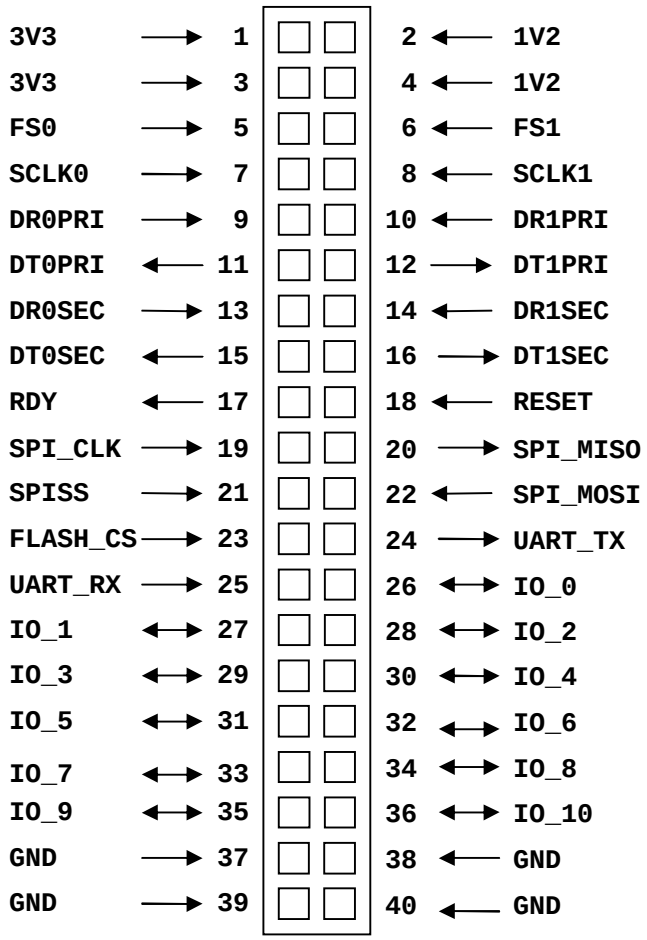

Figure 2. Connector Pin Diagrams

2 Features

Advanced signal processing:

- Subband echo cancellation (acoustic and line)
- Subband non-linear processing
- Comfort noise generation
- Stationary noise suppression
- Automatic gain control
- Dynamic range compression
- 32 uniform band frequency equalizer

Digital audio and control interfaces

- Two multi-channel PCM (TDM) digital audio interfaces
- A-law or µ-law companding according to G.711 specification
- SPI control

SPI configuration control:

- Programmable echo tail length (echo path capacity): 8-128ms

- **Programmable channel set configuration switching**
- **Maximal number of channels: 32**
- **Programmable companding low**

Scalable DSP performance:

ADSP-BF531/2/3 according to the number of channels

Special features:

- **Run time control SPI**
- **JTAG for DSP**
- **UART for test and debugging**
- **11 GPIO lines**

3 MEC^2 INTERFACES

3.1 PCM buses

MEC^2 connector incorporates two identical and independent serial PCM port buses A and B . Each bus consists of 6 lines. The names are similar to pin names of Blackfin serial port SPORT.
The standard software uses bus A (SPORT0) to receive /transmit audio data, only.
The line assignments in the standard software application described in Table 2.1:

TABLE 2.1: PCM BUS LINES

PCM A, SPORT0		PCM B, SPORT1[a)]		DESCRIPTION
Name	Pin	Name	Pin	
FS0	5	FS1	6	FS input signal is used for indicating the start of a block or frame of multi-channel input and output data words. Corresponding BF name is RFS [b)]
SCLK0	7	SCLK1	8	Input serial clock for input and output data bits. Corresponding BF name is RSCLK [c)]
DR0PRI	9	DR1PRI	10	Primary input data bits line
DT0PRI	11	DT1PRI	12	Primary output data bits line
DR0SEC	13	DR1SEC	14	Reference input data bits line
DT0SEC	15	DT1SEC	16	Reference output data bits line

Notes:
a) PCM B (SPORT1) is not used by the standard software
b) Blackfin TFS0 and TFS1 pins are not used in multifunctional mode. They are connected to control points at the board and used as "data valid" test signals active during receive/transmit time slots.
c) Blackfin TSCLK0 and TSCLK1 pins are not used in multifunctional mode.

SPI bus

SPI interface bus includes five lines described in Table 2.2.
The interface has various purposes. During the boot-loading period it is used to link boot flash memory and DSP.
During the Blackfin software runtime, SPI is used as a control interface, transferring commands from the system to MEC^2 and replays from MEC^2 to the system.
The system uses $\overline{\text{RDY}}$ line to differ the boot-load phase and software running phase.
While $\overline{\text{RDY}}$ is in high state, SPI bus is used inside the board and must be freed (tri-stated) at the system side.
The SPI interface also can be used for flash memory programming to load the memory with initial or update the software. For this purpose $\overline{\text{FLASH\_CS}}$ signal is present in the main connector pin.
At the time of flash programming DSP must be stopped by setting $\overline{\text{RESET}}$ line to zero.
The SPI data rate is defined by the system but can't exceed 10M Bauds.
Note, MEC^2 SPI is a slave device and the system is a master device both in control and flash programming modes.
SPI signal time diagrams for one control word transfer are shown in the Fig. 2.2.

TABLE 3.2: PCM BUS LINES

NAME	Pin	DESCRIPTION
SPI_CLK	19	SPI input serial clock signal
SPI_MISO	20	Data input pin, receiving input data
$\overline{\text{SPISS}}$	21	Active low SPI serial peripheral slave select input signal. It is used in

		control mode
SPI_MOSI	22	Data output pin, transmitting data to the system
$\overline{\text{FLASH\_CS}}$	23	Active low flash memory chip select signal. It is used for the memory writing

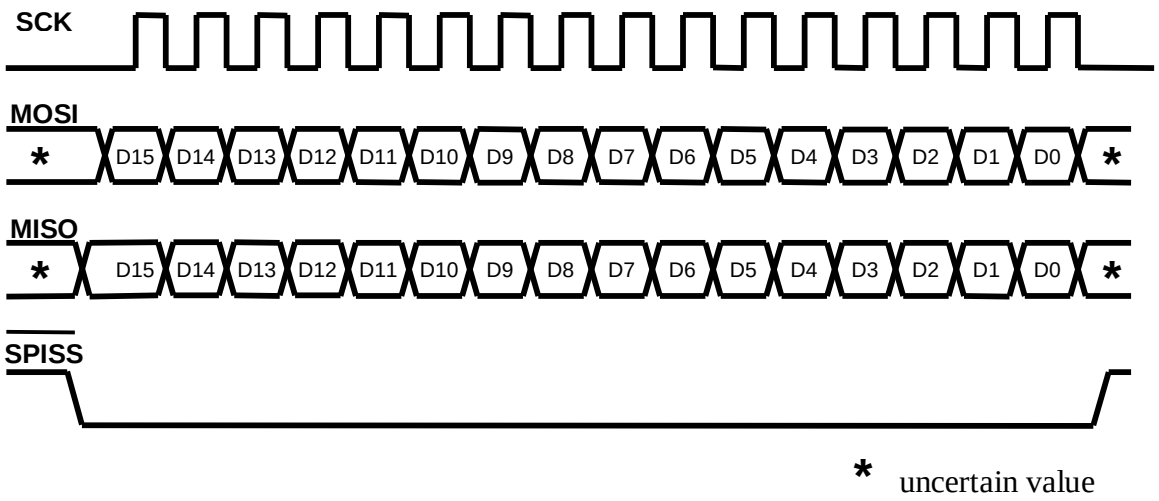

Figure 3.2. SPI Time Diagrams

UART interface

The standard software uses UART as a mean of data interchange between Blackfin DSP and PIC16F54 microcontroller. Therefore, UART lines must be in the high impedance state at the system side while the software runs.
But UART can be used with the special debug software for testing.
UART lines are described in Table 2.3:

TABLE 3.3: UART LINES

NAME	Pin	DESCRIPTION
TX	24	UART serial data output line
RX	25	UART serial data intput line

GPIO bus

Eleven General Purpose Input/Output lines are used in diverse ways. Their functions extensively depended on a system. Each line can be programmed as an input or output. Generally, input lines are used for modules serialization, providing MEC^2 with a unique hard-coded ID (so-called geographical address), and output lines are used for the module state reflection.
The standard software is not uses this bus, content itself with the single RDY line for active state indication.
GPIO lines have names IO_0…IO_10 and are brought out to pins 26..36 of the main connector.

Power supply lines

Power supply lines are redundant. They supplied the MEC² board with 1.2V for Blackfin DSP core and with 3.3V for all other circuits.
Power supply lines are tabled below:

TABLE 3.5: POWER SUPPLY LINES

NAME	Pin	DESCRIPTION
3V3	1	Common 3.3V power supply lines
3V3	3	
1V2	2	DSP core 1.2V power supply lines
1V2	4	
GND	37	System ground bus
GND	38	
GND	39	
GND	40	

4 STANDARD SOFTWARE

The standard MEC² program performs multi-channel processing including:

- Echo Canceller (EC) with controlled echo tail length parameter from 8 ms to 128 ms
- Static Noise Suppressor (SNS)
- Subband non-linear processing
- Comfort noise generation
- Automatic Gain Control (AGC)
- Dynamic Range Compressor (DRC)
- Multi-Band Equalizer (MBE)

The program allows communicating in a Time-Division-Multiplexed (TDM) serial system. It is assumed that two input lines DR0PRI and DR0SEC carry the primary (S_{IN}) and reference (R_{IN}) data flows, correspondently. Result signals form data flows on two output lines DT0PRI (S_{OUT}) and DT0SEC (R_{OUT}), correspondently.
The flows are a series of data frames. The beginning of every frame is signaled by frame sync FS0, and every bit of data is accompanied by bit clock signal SCLK0.
The flow frame consists of time slots with eight bit duration, most bit first. Such slot contains one word of companding data. The companding low can be selected either G.711 μ-law or G.711 A-law by software for all data, totally.
The primary signal and the reference signal for a single audio channel share the same time slot. In other words, this couple of signals incomes to input data lines DR0PRI and DR0SEC simultaneously.
Resulting output signals from an audio channel share the same time slot with the corresponding input signals. So one digital audio channel occupies one time slot.
The maximum 32 digital audio channels can be picked out from any 128 contiguous channels out of the 1024 total channels for passing through the MEC² board.
Every separate channel processing can be set on or off during the software running without another channel processing suspending.

4.1 SPI control interface

The processing configuration is controlled by commands. The system send to the MEC² software 16-bits commands sometimes accompanied with additional data words via SPI bus described in 2.2. section.

4.1.1 Command word format

The command format is:

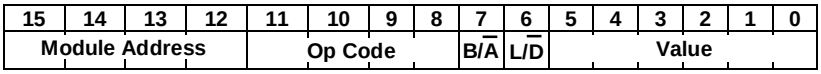

Figure 4.1.1. Command Format

The system can include up to 15 MEC² modules. A four-bits Module Address field specifies a destination module for the command.
The binary address 0000 is a "broadcast" address that match for any module. It useful either for sending common commands for all MEC² modules or to refer a module that has individual SPISS line.
Therefore, the system can destine commands to separate 15 modules with addresses from 1 to 15.

4.1.2 Op Code field

The four-bits field Op Code can be one of following:

TABLE 4.1.2: Defined opcode meanings

Op Code	Name	Meaning
0	No Operation	Does nothing. Useful for reply receiving
1	Version	Query of MEC² SW version
2	Reset	Set default settings
3	Companding	Set type of companding
4	Tail	Set cancelled echo tail length
5	Window	Set channel window position and size
6	Pattern	Set bit pattern of received/sent channels
7	EC ON/OFF	Set processing of certain channel on/off
8	Reply ON/OFF	Set module reply mode on/off
9	Resume	Start processing after suspending

4.1.3 B/$\overline{A}$ field

The field points the PCM bus in commands that can have different settings for different PCM buses. At a moment these commands are Window, Pattern, and EC ON/OFF.
0 means that command is directed to PCM A bus, 1 means that command directed to PCM B.
Though the field is destined, in standard software it always has the value 0, because the software does not use PCM B.

4.1.4 L/$\overline{D}$ field

The L/$\overline{D}$ fields indicates usage of the next field, Value.
When L/$\overline{D}$ field is 0, Value field either is empty or contains data value.
When L/$\overline{D}$ field is 1, Value field contains the number of additional data words that follow the command.

4.1.5 Value field

The field carries a number that is either a data value or number of following data words depending on L/$\overline{D}$ field content. The field assignments are discussed below in details.

4.1.6 Version command

Version command inquires MEC^2 module about software version.
In addition to direct purpose the command is useful for module connection testing, because the command always must be replied by the module.
The fields B/$\overline{A}$, L/$\overline{D}$, and Value have no meaning.
The command does not suspend processing.

4.1.7 No Operation command

The command is used when the system tries to get reply on a previous sent command from MEC^2. The module ignore this command in essence, but SPI hardware uses the command clocks for reply sending.
The command does not suspend processing.

4.1.8 Reset command

The command set all default settings restarting software.
The fields B/$\overline{A}$, L/$\overline{D}$, and Value have no meaning.

4.1.9 Companding command

The command set type of data companding.
'0' in Value field means G.711 A-law companding, '1' means G.711 μ-law companding.
The companding always the same for both PCM buses.
The field B/$\overline{A}$ is of no use. The field L/$\overline{D}$ is equal to zero.
The command execution concerned with hardware reset and suspends MEC^2 processing.

4.1.10 Tail command

Tail command set echo tail cancellation length (echo pass volume).
Value field codes point required tail length:

TABLE 4.1.10: Echo tail codes

Value	Tail length, ms
0	8
1	16
2	32
3	64
4	128

The fields B/$\overline{A}$ is of no use. The field L/$\overline{D}$ is equal to zero.
The command requires software reconfiguration and suspends MEC^2 processing.

4.1.11 Window command

The command specifies position and size of channel window out of the 1024 total channels. The format of this command parameters is the same that used for Blackfin SPORT programming. The command parameters is 16-bits long and placed to the data word followed the command:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Window Size Code				N/A		Window Offset									

Figure 4.1.11. Data Word Format for Window Command

To calculate Window Size Code from a number of contiguous channels use the equation:

Window Size Code = (Number of Channels + 7) / 8 – 1,

where Number of Channels has a range from 1 to 128.
Window offset specifies where in the 1024-channel range to place the start of the window. A value of 0 specifies no offset and 896 is the largest value that permits using all 128 channels.
B/$\bar{A}$ field shows goal PCM bus. The field L/$\bar{D}$ is '1' and Value field is 1, since command is followed by one data word.
The command suspends MEC^2 processing.

4.1.12 Pattern command

The command is followed by eight data words. Each of the eight words has 16 bits, corresponding to 16 channels. Setting a bit enables that channel, MEC^2 selects its channel from the multiple channels.
Data bits are enumerated in ascended order. The least bit 0 of the first data word corresponds to the first channel of the window. The most bit 15 of the eighth word corresponds to the 128 channel of the active window.
B/$\bar{A}$ field shows goal PCM bus. The field L/$\bar{D}$ is '1' and Value field is 8, corresponding to number of additional data words.
The command suspends MEC^2 processing.

4.1.13 EC ON/OFF command

The command can set the processing of a specified channel on or off.
For this command Value field is divided on two parts: Act and Channel No:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Module Address				0	1	0	1	B/$\bar{A}$	0	Act	Channel No				

Figure 4.1.12a. EC ON/OFF Command Format

Act field points the desirable state of the channel. '1' corresponds to processed channel, '0' corresponds to channel without a processing.
Channel No field is a number of a channel in a set of channels that are marked with '1' in the data word of Pattern command, starting from 0.
Suppose, for example, the channel window offset is 7 and the first data word of Pattern command is equal to 0x4FE5.
In the total 1024 channel flow the addressed with the Channel No is equal to 5 channel has the number 15:

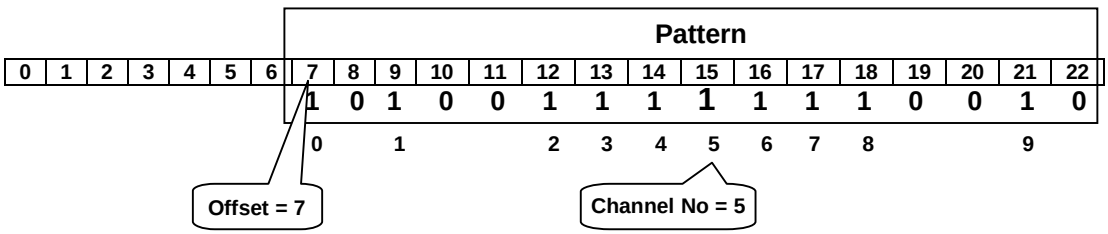

Figure 4.1.12b. Channel No selection example

B/$\bar{A}$ field shows goal PCM bus. The field L/$\bar{D}$ is 0.
The command does not suspend processing.

4.1.14 Reply ON/OFF command

MEC^2 module can be turned to Reply mode. In this mode MEC^2 answers on every command with the reply word. The Reply mode is useful during debug and test stages.
The system can get reply information sending the next word via SPI interface. The system can send the dummy command No Operation if it does not need in sending any effecting command.
The format of Reply word is the same as a format of received command, but Value field change its meaning:

TABLE 4.1.14: Reply codes

Code	Name	Meaning
0	Successful	The command executed successfully
1	Unknown	Op code is not supported
2	Busy	Command can't be done at a moment
3	Bad parameter	The data field value is unsupported
4	Version	ID of module software version

The Reply command can turn this mode on or off.
0 in Value field turns Reply mode off, 1 turns Reply mode on.
The fields B/$\overline{A}$ and L/$\overline{D}$ have no meaning.
The command does not suspend processing.

4.1.15 Resume command

The command intended for resumption of work when all necessary parameters are changed.
The fields B/$\overline{A}$, L/$\overline{D}$, and Value have no meaning.

5 Cost of components estimation

The material list includes component prices of Digikey catalog as on January 2008, on the basis of 1000 production lot. ADSP Blackfin cost is not included. It can be obtained from Analog Devices Inc. or its distributers:
http://www.analog.com/en/epProd/0,,ADSP-BF531,00.html#price,
http://www.analog.com/en/epProd/0,,ADSP-BF532,00.html, and
http://www.analog.com/en/epProd/0,,ADSP-BF533,00.html for ADSP BF531, ADSP BF532, and ADSP BF533 correspondently and has the range $10-$20.
Prices are in US dollars.

TABLE 5: MEC^2 materials

Item	Quantity	Reference	Nominal	Price	Cost
1	4	Capacities	10.0uF	0.16	0.64
2	22	Capacities	0.01uF	0.02	0.44
3	1	Capacity	0.1 uF	0.02	0.02
4	1	LED S530-A2		0.09	0.09
5	1	Ferrite bead	120 W	0.005	0.01
6	1	Header 2x7		0.16	0.16
7	12	Resistor arrays	33 W	0.031	0.37
8	2	Resistors	33 W	0.005	0.01
9	1	Resistor	0 W	0.005	0.01
10	1	Resistor	330 W	0.005	0.01
11	1	SDRAM MT48LC8M16A2P	7.5 ns	3.51	3.51
12	1	uController PIC16F54		0.47	0.47
13	1	Serial flash RAM M25P05	128Mb	1.34	1.34
14	1	Cristal oscillator	25 МГц	1.07	1.07
TOTAL:					8.14